SEMICONDUCTOR DEVICE FITTED WITH CERAMIC HEAT-RADIATING FINS

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Inventor(s): KAWASHIMA MASAMI
Applicant(s):: TOKIN CORP
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Equivalents:

Abstract

PURPOSE:To miniaturize a device and to improve heat radiation efficiency by constituting a substrate fitted with ceramic heat radiating fins so that it may sandwich a semiconductor element from both sides of it.
CONSTITUTION:This is put in such structure that a semiconductor element 5 is sandwitched from both sides by high heat conductive ceramics, and heat radiating fins 10 are formed at one side of the ceramic, and a semiconductor element 5 is mounted directly on the smooth face of the ceramic. And the heat generated from the semiconductor element 5 is radiated in two directions from the two sides of the semiconductor element 5 directly through the ceramic. Hereby, heat radiating effect becomes large, and a semiconductor device of large output can be miniaturized as compared with the conventional structure.

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⑫公開特許公報(A)　平3−20067

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審査請求　未請求　請求項の数 3　(全5頁)

㊹発明の名称　セラミック放熱フィン付半導体装置

㉑特　願　平1−111167

㉒出　願　平1(1989)4月29日

㉜発明者　川島　正実　宮城県仙台市太白区郡山6丁目7番1号　株式会社トーキン内

㉛出願人　株式会社トーキン　宮城県仙台市太白区郡山6丁目7番1号

明細書

1　発明の名称

セラミック放熱フィン付半導体装置

2　特許請求の範囲

1.一方の面に放熱フィンを形成し、もう一方の面には金属導体パターンが形成された絶縁性セラミック基板2個の間に、少なくとも1個の半導体素子をサンドイッチ状に挟持し、前記半導体素子の電極端子を、それぞれ前記2個の絶縁性セラミック基板の導体パターンと導通させ、しかも該セラミック基板に外部回路へ接続する所定の端子が形成してあることを特徴とするセラミック放熱フィン付半導体装置。

2.前記絶縁性セラミック基板の少なくとも1個を、窒化アルミニウムにより形成した事を特徴とする請求項1記載のセラミック放熱フィン付半導体装置。

3.2つの絶縁性セラミック基板の間の半導体素子の、電極付前記絶縁性セラミック基板上に形成した導体パターンとの間にうす板の半田をおき、2つの絶縁性セラミック基板の間を決める長さのスペーサを持つ連結ボルトにより2つの絶縁性セラミック基板を固定した後、昇温して2つの絶縁性セラミック基板、半導体素子、基板上のスペーサを半田により固定したことを特徴とする請求項1、請求項2記載のセラミック放熱フィン付半導体製造装置。

3　発明の詳細な説明

イ．発明の目的

〔産業上の利用分野〕

本発明は電力増幅を目的に使用する電力増幅回路を構成する半導体装置において、熱伝導性に優れたセラミックを用い、セラミック放熱フィンを形成したセラミックス基板と、半導体素子とを一体に構成したセラミックス放熱フィン付半導体装置に関する。

〔従来の技術〕

従来、発熱を伴うパワートランジスタ、MOSIC等の、電子機器に実装する電力増幅回路に使用される半導体素子は、金属ケースに実装し、電気絶縁材を介して熱伝導と放熱性に優れた金属のアルミニウム等を用い、作ったフィンを取り付けて、半導体装置の放熱が行なわれている。また、放熱フィンは、半導体素子の接合面側、即ちコレクタ側又はドレン側に1個取り付けられ、コレクタ側又はドレン側の一方向のみへの熱伝導による放熱構造がとられている。近年、半導体素子の高性能化、高密度化の傾向が進み、それに伴い素子の単位面積当たりの発熱量も増してきており、装置を小形化する目的から放熱効率のよい半導体装置が要求されている。

従来の技術において、半導体素子より発生した熱は、有機フィルム等熱伝導性に劣る絶縁シートを介し、半導体素子を納めた金属ケースをアルミニウム等のフィンに実装しているため、放熱方向は絶縁シート側一方向のみであり、介在する絶縁シートにより熱抵抗が増加し、放熱特性が悪いという問題を有していた。

〔発明が解決しようとする課題〕

本発明は、前記の課題に対し、半導体素子から発生する熱を、金属アルミニウムと同様な熱伝導率を有する、窒化アルミニウム、炭化珪素、酸化ベリリウムで代表される高熱伝導性セラミックにより、半導体素子を両面からサンドイッチにする構造にして、セラミック片面に放熱フィンを形成し、該セラミックの平滑な面に半導体素子を直接実装する構造とし、半導体素子より発生する熱を直接セラミックを介して半導体素子の2面より2方向に放熱させるよう構成したセラミック放熱フィン付半導体装置を提供することを目的とする。

ロ．発明の構成

〔課題を解決するための手段〕

前記目的を達成するために、本発明におけるセラミック放熱フィン付半導体装置は、発熱に伴う半導体素子を実装するための配線基板として、窒化アルミニウム、炭化珪素、酸化ベリリウム等の高熱伝導性セラミックを用いる。

これらのセラミックは、熱伝導率が200W/mkないし270W/mk前後と、熱伝導率が240W/mk程度の金属アルミニウムとほぼ同程度の熱伝導特性を有し、しかも電気絶縁体である。これらのセラミック基板表面にそれぞれのセラミックに適するメタライズ手法により配線パターンを設け、半導体装置の実装基板とし、周辺回路と接続可能な構造とする。

本構造のセラミック放熱フィン付基板を半導体素子の両側からサンドイッチとなるように構成することにより、半導体素子より発生する熱を半導体素子両面より直接セラミック放熱フィン付基板へ逃がすことが出来るようにするものである。

即ち本発明は、

1.一方の面に放熱フィンを形成し、もう一方の面には金属導体パターンが形成された絶縁性セラミック基板2個の間に、少なくとも1個の半導体素子をサンドイッチ状に挟持し、前記半導体素子の電極端子を、それぞれ前記2個の絶縁性セラミック基板の導体パターンと導通させ、しかも該セラミック基板に外部回路へ接続する所定の端子が形成してあることを特徴とするセラミックス放熱フィン付半導体装置である。

2.前記絶縁性セラミック基板の少なくとも1個を窒化アルミニウムにより形成した事を特徴とする請求項1記載のセラミック放熱フィン付半導体装置である。

3.2つの絶縁性セラミック基板の間の半導体素子の電極付前記絶縁性セラミック基板上に形成した導体パターンとの間にうす板の半田をおき、2つの絶縁性セラミック基板を挟める間の長さのスペーサを持つ連結ボルトにより2つの絶縁性セラミック基板を固定した後、昇温して2つの絶縁性セラミック基板、半導体素子、基板上のスペーサを半田により固定したことを特徴とする請求項1、請求項2記載のセラミック放熱フィン付半導体製造装置である。

〔作用〕

高出力特性の半導体素子を、放熱フィンの形に加工した高い熱伝導率特性を持つ窒化アルミニウ

ム、炭化珪素、酸化ベリリウムのセラミックの面に電極パターン、並びに導体パターンを取付け、半導体素子のドレン面をセラミックの面に半田によりリフロー溶接を行い、一方半導体素子のソース電極面は、一方の放熱フィン付セラミックの上に形成したソース電極パターンに接触させ、2つの放熱フィン付セラミックは4隅にあけた連結用穴を用い、中央に半導体素子と電極パターン、半田層等の各部品の合計長さのスペーサを取付け、両側にねじ取付けた連結ボルトを通し、ナットにより固定する構造のセラミック放熱フィン付半導体装置とする。従って従来のパワー用半導体装置では金属製放熱フィンとの間には電気絶縁のための樹脂製フィルムを挿入し又半導体素子と金属ケースの間の接続にモリブデン板等を用いていたのに対して、半導体素子のドレン電極、並びにソース電極は、電極パターンのみであり、高い熱伝導特性を持つ放熱フィン付セラミックに前記ドレン電極とソース電極が直接接触する構造であるので、半導体素子に発生する熱は、直接セラミックスの放熱フィンに伝達される。一方半導体素子と電極パターンは、金属棒の中央に、半導体素子、半田層、導体パターンの厚さの合計に相当する一体構造のスペーサを取り付けた連結ボルトにより組立て固定する構造であるので、半導体素子に応力による歪を与えることはない。又半導体素子の各電極パターンは、放熱フィン付セラミックの下面に導き出されており、直接基板導体に接続される構造としてある。

〔実施例〕

本発明の実施例について図面を参照し、詳細に説明する。

第1図は本発明によるセラミック放熱フィン付半導体装置の平面図であり、第2図は本発明によるセラミック放熱フィン付半導体装置の正面図であり、第3図はセラミック放熱フィン付半導体装置の半導体素子を実施した面の平面図、第4図はソース電極を取り付けたセラミック放熱フィンの平面図を示す。高い熱伝導特性を有するセラミックで作られた半導体素子を実装する窒化アルミニウム放熱フィン付基板1a、1bは、本発明の実施例では粒径が1μm以下の窒化アルミニウム原料粉に、酸化イットリウムを3重量%添加して混合を行い、得られた混合粉末にポリブチルブチラール(PVB)をバインダーとして添加し、乾式プレス法により1 ton/cm^{2}の圧力で成形体を作る。成形体を500℃に於て除々にバインダーを除去した後、非酸化性雰囲気中、例えば窒素ガス、又はアルゴンガス雰囲気中で1850℃で5時間の焼結を行い、窒化アルミニウム放熱フィン付基板の焼結体ブロックを得る。放熱フィンは研削により溝10を形成する。

ついで、電極パターンを形成する面を研摩した窒化アルミニウム放熱フィン付基板1aの面に、半導体装置の電極を形成するためのドレン電極パターン2aを、窒化アルミニウム放熱フィン付基板1bの面にはソース電極パターン2cを形成する。窒化アルミニウムフィン付基板に銅層を主層とするドレン電極パターン2a、ゲート電極パターン2b、ソース電極パターン2cを形成する手段は、本発明の発明者等によりすでに出願されている昭和63年特許願第21025号の手法による。

各電極パターンの構成はその概要を述べると、ニッケル無電解メッキ層を3μmないし5μm窒化アルミニウム面に形成後、電気メッキにより銅層の厚さをほぼ100μmの厚さにメッキして形成し、銅メッキ層の上にニッケルに微量のボロンを添加した合金層を数μmの厚さに形成し、一部に必要に応じ鉛－錫共晶半田被覆を施す。ついで第3図に示す形状にドレン電極パターン2a、ゲート電極パターン2bを、第4図に示す形状のソース電極パターン2cを設け、ドレン電極パターン2a上に本発明では静電誘導トランジスターの半導体素子5のドレン電極を接続した。

通常パワー用の半導体素子は、ドレン側にメタライズ層を形成した半導体素子をモリブデン板等にろう付けし形成されるが、本発明ではセラミック表面に形成された電極パターンのドレン電極パターン2a上に、半導体素子底面のドレン部と同じ大きさで、厚みが50μmの半田薄板を切断して設

置し、半導体素子の上から荷重を加えながら350℃でリフロー半田溶接を行った。

ついで、第3図に示すように半導体素子5のゲート電極4bと、セラミックの導体パターンのゲート電極パターン2bを、直径50μmのアルミ線を用い超音波ボンディングにより接続した。尚、ドレン電極パターン2a及びゲート電極パターン2bは、本半導体装置をプリント基板等の表面に実装する際、プリント基板側の配線パターンとの接合を容易にするため、プリント基板対向面の導体パターン2a-1、2b-1、2c-1には、あらかじめ30μm前後の厚みで鉛－錫共晶半田メッキによる塗装を施した。一方、半導体装置のソース部に対向するソース電極パターン2cは、同様の手法にて他方の窒化アルミニウム放熱フィン付基板1bのセラミック表面に形成され、予め導体表面は30μm前後の鉛－錫共晶半田により被覆を施した。そして、ドレン電極パターン、接合半田層、ドレン電極パターン、半導体素子、ゲート電極パターン、ソース電極パターンの積層厚さに相当したスペーサ8aを取り付けた連結ボルト9を用いて組立て、第1図、第2図に示すように連結ボルトの両側ボルト部分を窒化アルミニウム放熱フィン付基板四隅の連結用孔に通し、ナットにより2つの窒化アルミニウム放熱フィン付基板を連結し固定する。従って半導体素子のソース電極パターン2cに半田付け、又はろう付けを行うことなく接触のみで接続する。又このようにして形成された1組みのセラミック放熱フィン付半導体装置は、270℃でリフロー炉を通過させ半導体素子のソース電極パターン2cと導体パターン2c-1を半田接合する。最後に耐湿性を考慮して2つのセラミック放熱フィン付基板の間を被覆樹脂7より完全に覆い固化し、半導体素子、ジャンパー線、電極パターンを覆い完成する。樹脂としては日本チバガイギー株式会社製半導体チップのコーティング樹脂、XNR5100、XNH5100等を用いれればよい。

尚、本発明の実施例は窒化アルミニウムの例により説明したが、熱伝導特性に優れたセラミックである窒化アルミニウム以外の、炭化珪素、酸化ベリリウム等を用いた組合せも、本発明と同様なセラミック放熱フィン付半導体装置を形成し得ることは当然である。又窒化アルミニウム表面に形成する金属層は、薄い銅層を例に説明したが、ニッケルメッキ、金属アルミニウムや他の金属層を形成してもよい。

ハ．発明の効果

〔発明の効果〕

本発明は以上に説明したように構成されているので、以下に記載されるような効果を奏する。

半導体素子は、金属アルミニウムと同じ熱伝導特性を有し、しかも電気絶縁特性を持つ放熱フィン付セラミックに半導体素子をマウントし金属ケースを介さずに一体化した実装構造とし、半導体チップの両面に放熱フィンを構成した構造となっているため、放熱効果が極めて大きく、従来の構造に比較して大出力の半導体装置を小型化して提供できる。

以下余白

4　図面の簡単な説明

第1図は本発明によるセラミック放熱フィン付半導体装置を示す平面図。

第2図は本発明によるセラミック放熱フィン付半導体装置を示す正面図。

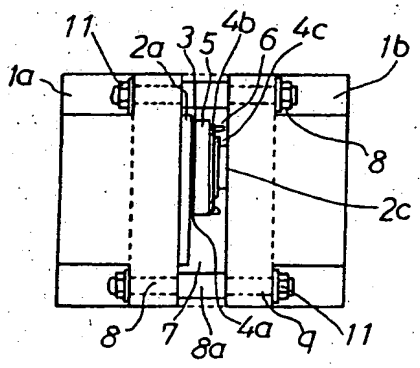
第3図は第1図における窒化アルミニウム放熱フィン付基板1aの半導体素子搭載面の平面図。

第4図はソース電極パターン形成面の平面図。

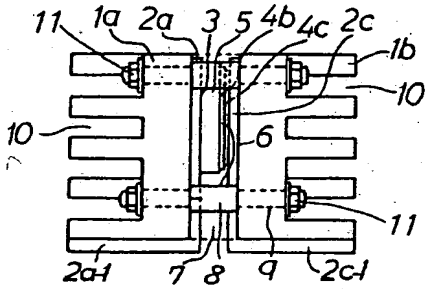
1a,1b…窒化アルミニウム放熱フィン付基板、2a…ドレン電極パターン、2b…ゲート電極パターン、2c…ソース電極パターン、2a-1,2b-1,2c-1…導体パターン、3…シリコンチップ接合半田層、4a…ドレン電極、4b…ゲート電極、4c…ソース電極、5…半導体素子、6…ジャンパー線、7…被覆樹脂、8…ナット、8a…スペーサ、9…連結ボルト、10…溝、11…ナット。

特許出願人　株式会社トーキン

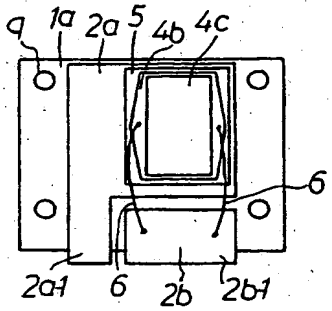
第 1 図



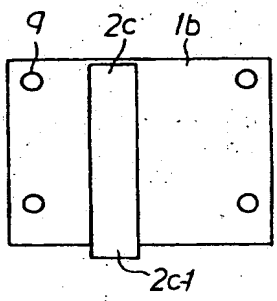
第 2 図



第 3 図



第 4 図



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H01L 23/02

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(56) Documents cited
None

(58) Field of search
H1K

(71) Applicant
General Electric Company (USA–New York),
1 River Road, Schenectady, 12305 State of New York,
United States of America

(72) Inventors
Alexander John Yerman
Constantine Alois Neugebauer

(74) Agent and/or Address for Service
Brookes & Martin,
High Holborn House, 52/54 High Holborn, London
WC1V 6SE

(54) Hermetic power chip packages

(57) A hermetic power chip package comprises a dielectric plate (18) having at least a first electrode (20, 22, 24) bonded to a lower surface of the plate, a corresponding conductive lead bonded to an upper surface of the plate, and at least one conductive through hole interconnecting the electrode and the lead, a power chip (16) having at least a first terminal (34, 36) on its upper side bonded to the first electrode and a terminal (38) on its lower side, and a lower electrode (17) in the form of a conductive sheet bonded to the lower terminal (38) and hermetically sealed to the dielectric plate 18 through a metallic sealing ring (42).

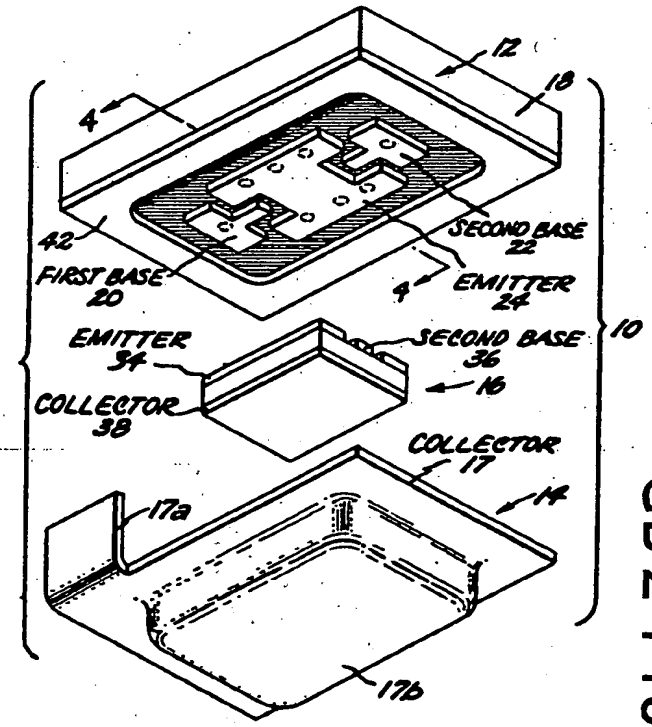

FIG. 1

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FIG. 1

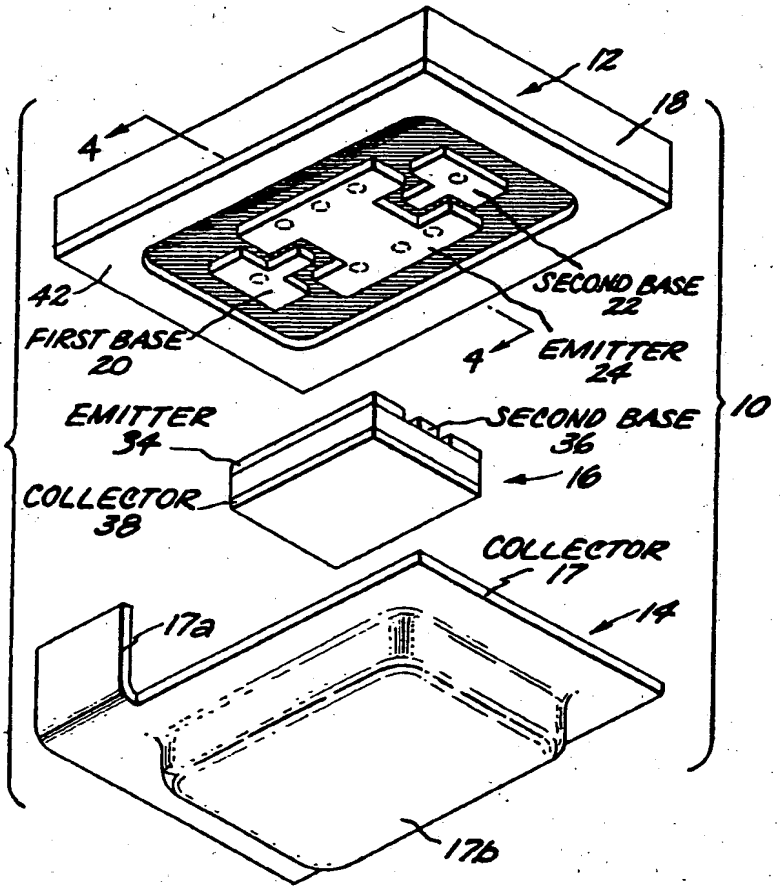


FIG. 4

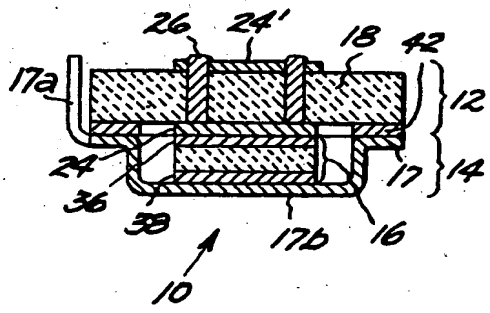


FIG. 5

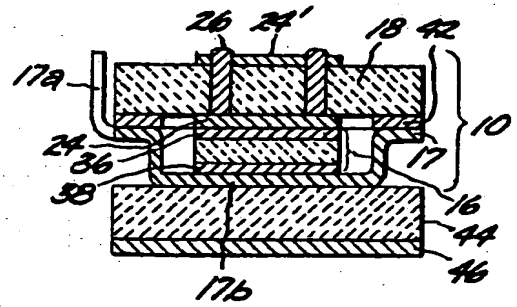


FIG. 2

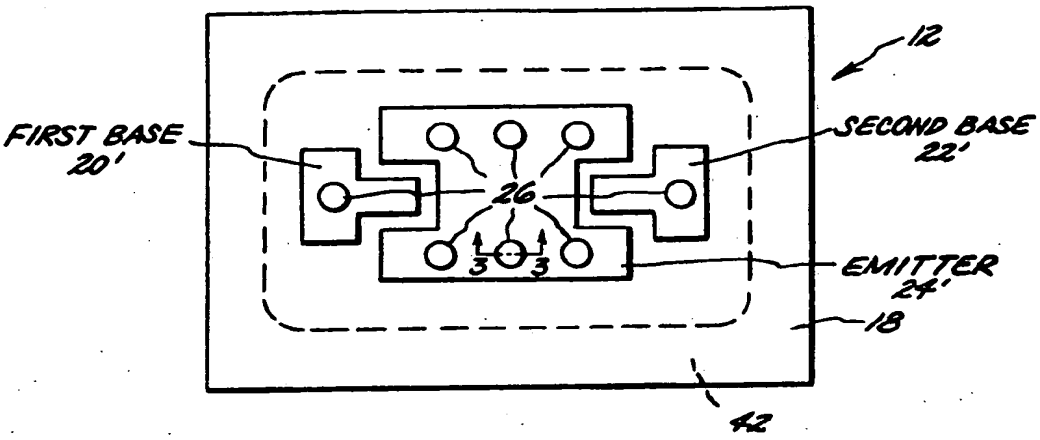


FIG. 3

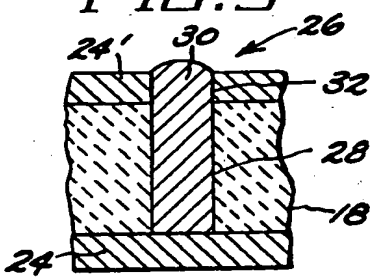
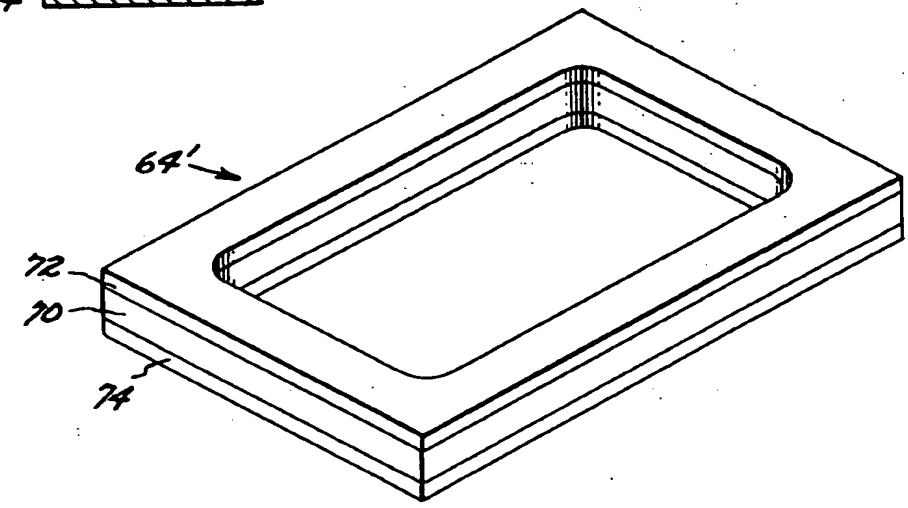


FIG. 8



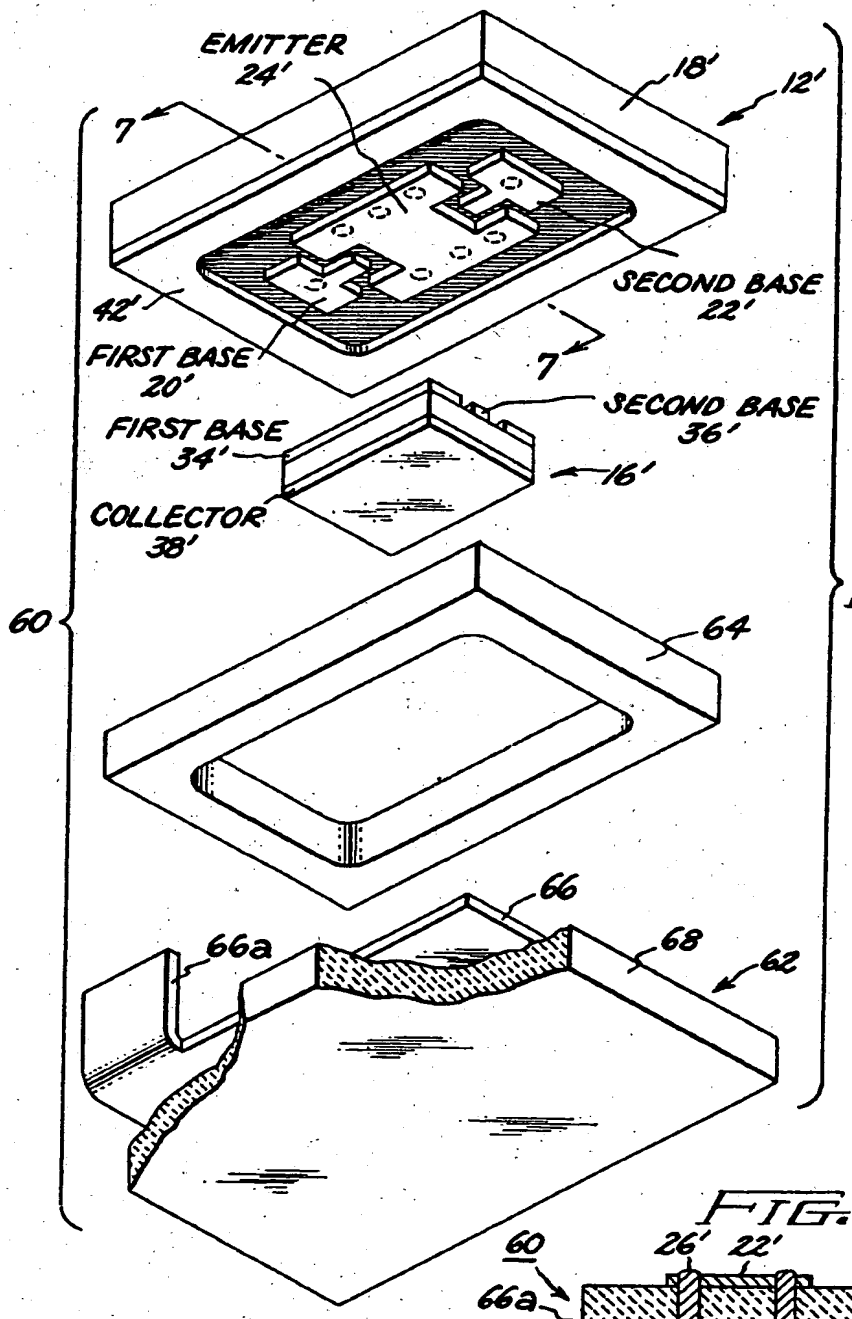

EMITTER
24'
18'
12'
7
7
42'
SECOND BASE
22'
FIRST BASE
20'
SECOND BASE
36'
FIRST BASE
34'
16'
COLLECTOR
38'
60
64
66
66a
68
62

FIG. 6

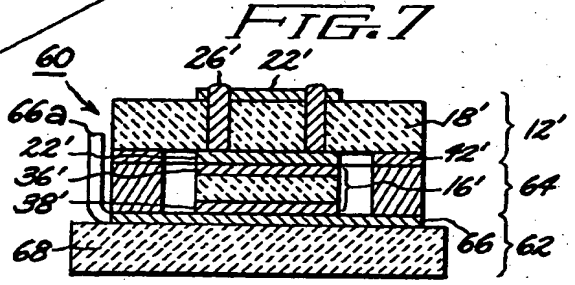

60
26'
22'
66a
18'
12'
22'
42'
36'
16'
64
38'
68
66
62

FIG. 7

SPECIFICATION

Hermetic power chip packages

The present invention relates to packages for power semiconductor chips, and, more particularly, to hermetic power chip packages.

Power semiconductor chips (hereinafter, simply "power chips") generate waste heat during operation typically in excess of about one watt. This heat must be removed in order to prevent destruction of the power chip. Power chips are accordingly assembled in a package or arrangement designed to facilitate the removal of heat from the power chip. Hermetic, or airtight, packages are particularly desirable for packaging power chips, since hermetic packages shield the power chips from contaminants and moisture that are known to degrade the operating performance of power chips.

A typical hermetic power chip package that is presently available includes a relatively massive metallic baseplate on which the power chip is thermally mounted, and, which, in turn, is adapted to be thermally mounted upon a metallic heat sink. Two glass-to-metal hermetic seals are typically incorporated in the power chip package to permit electrical access to the power chip via current leads. These glass-to-metal seals are expensive to make, and the use of the metallic baseplate is also expensive. The power chip package additionally includes a housing that hermetically encloses the power chip and one or more of the foregoing glass-to-metal seals resulting in further expense of the package.

The foregoing describes a hermetic power chip package in an essentially completed form, that is, in a form ready for use in circuit applications. Initial electrical testing of power chips has heretofore been carried out by assembling the power chips in completed hermetic power chip packages to provide for removal of waste heat. Such testing is necessary to ascertain important device characteristics, such as, in a power Darlington transistor, the common emitter current gain, H_{FE}, and the collector-to-emitter voltage at device saturation, $V_{CE(SAT)}$. If the power chip in a power chip package does not meet the required standards, the entire power chip package is discarded. As a consequence, the testing of power chips in presently available hermetic packages is costly. In order to make testing of power chips more economical, it would be desirable to provide a hermetic power chip package in a partially-completed or building block form, so as to reduce the expense of discarded packages.

Accordingly, an object of the present invention is to provide a relatively inexpensive hermetic power chip package having a high capacity for heat removal from a power chip, particularly a package that is dielectrically isolated from a heat sink on which the hermetic power chip package may be mounted, and which is in building block form.

A further object of the invention is to provide a hermetic power chip package that does not require the inclusion of a metallic baseplate for power chip testing.

In accordance with the present invention, there is provided a hermetic power chip package, which, in a preferred form as directed to a power Darlington transistor, includes an upper package section, a power Darlington transistor, and a lower package section. The upper package section comprises a dielectric plate with first and second base electrodes and an emitter electrode on the underside thereof. Electrical access to these electrodes is provided from the top side of the dielectric plate by corresponding first and second base leads and an emitter lead, which leads are respectively connected through the dielectric plate to the first and second base electrodes and the emitter electrode via vertically-oriented conducting-through holes in the dielectric plate. The upper package section further includes a metallic sealing ring bonded to the underside thereof and encompassing the first and second base electrodes and the emitter electrode.

The power Darlington transistor has first and second base terminals and an emitter terminal on the upper side thereof, which are electrically connected to the corresponding electrodes on the underside of the dielectric plate of the upper package seciton, and also has a collector terminal on the lower side thereof.

The lower package section comprises a collector electrode that is bonded to the single collector terminal and, additionally, that is bonded to the metallic sealing ring of the upper package section so as to hermetically enclose the power Darlington transistor.

The foregoing hermetic power chip package does not require a metallic baseplate and is in a partially completed or building block form.

A further hermetic power chip package in accordance with the present invention as directed to a power Darlington transistor, incorporates an upper package section and a power Darlington transistor that are suitably identical to the corresponding parts of the power chip package just described. The further package includes a lower package section comprising a collector electrode in sheet form bonded to the upper side of the plate, and which electrode, in turn, is bonded to the lower or collector terminal of the power Darlington transistor. A gasket is disposed between the upper and lower package sections, with the upper side of the gasket being bonded to the metallic sealing ring of the upper package section and the lower side of the gasket being bonded to the collector electrode of the lower package section. The ther-

mal expansion coefficient of the gasket is preferably selected to be within about ± 50 percent of that of the upper package section. The resulting package can undergo repeated cycling between widely differing hot and cold temperatures and yet maintain mechanical integrity and hermeticity.

In the accompanying drawings, by way of example only:–

Figure 1 is an exploded view of power chip package looking upward towards the power chip package, in accordance with the invention;

Figure 2 is a top plan view of upper package section 12 of Fig. 1 shown somewhat enlarged;

Figure 3 is a detail view in cross-section of a conducting-through hole 26 of Fig. 2 taken along line 3–3 of Fig. 2;

Figure 4 is a cross-sectional view of the power chip package of Fig. 1 when assembled, taken along line 4–4 of Fig. 1;

Figure 5 is a view similar to Fig. 4, illustrating an alternative embodiment to the power chip package of Fig. 1;

Figure 6 is an exploded view of a power chip package, looking upward towards the power chip package;

Figure 7 is a cross-sectional view of the power chip package of Fig. 6 when assembled, taken along line 7–7 of Fig. 6; and

Figure 8 is a depiction of an alternative implementation of gasket 64 of Fig. 6.

There is shown as Fig. 1 an exploded view of a hermetic power chip package 10 looking upward towards package 10, in accordance with the present invention. Package 10 comprises upper and lower package sections 12 and 14 with an exemplary power chip 16 situated therebetween, such as a power Darlington transistor.

Upper package section 12 comprises a dielectric plate 18 with a thermal expansion coefficient close to that of power chip 16, for example the ceramic beryllia or alumina where power chip 16 comprises silicon. Bonded to the lower side of dielectric plate 18 are first base electrode 20, second base electrode 22 and emitter electrode, 24. These electrodes preferably comprise copper that has been bonded to dielectric plate 18 by a eutectic bonding procedure; that is, a bonding procedure during which a molten eutectic alloy is formed between each of electrodes 20, 22 and 24 and dielectric plate 18. Details of preferred eutectic bonding procedures are discussed (and claimed) in the following U.S. Patents: No. 3,766,634—G.L. Babcock et al., issued 23 October 1973 and No. 3,994,430—D.A. Cusano t al., issued 30 November 1976. These pat nts are assigned to the present assignee and their ntire disclosure are incorporated h rein by reference. As an alternative to using eutectically bonded copper for electrodes 20, 22 and 24, these electrodes may compris metallic she ts, such as copper, that are soldered to a solderable metal layer (not shown) that is deposited onto the underside of dielectric plate 18, such as by evaporation of copper onto plate 18.

On the upper surface of dielectric plate 18, as shown in the enlarged top plan view of Fig. 2, a set of leads is provided that is complementary to electrodes 20, 22 and 24, that is, first base lead 20′, second base lead 22′ and emitter lead 24′. These complementary leads 20′, 22′ and 24′ provide electrical access from the exterior of power chip package 10 to electrodes 20, 22 and 24, which are located in the interior of power chip package 10.

Electrically interconnecting interior electrodes 20, 22 and 24 (Fig. 1) with exterior electrodes 20′, 22′, and 24′, as illustrated in Fig. 2, are conducting-through holes 26, indicated in Fig. 1 by dashed lines. A suitable construction of a conducting-through hole is illustrated in the detail view of Fig. 3, taken along lines 3–3 in Fig. 2, and which is in fragmentary, cross-sectional form. As can be observed in Fig. 3, a hole 28 is provided vertically through dielectric plate 18, which is filled with a conduting medium, such as solder 30. In a preferred procedure for forming conducting-through hole 26, hole 28 is first provided in dielectric plate 18, followed by the bonding of emitter electrode 24 to the underside of dielectric plate 18. Electrode 24 covers the bottom of hole 28 so as to hermetically seal hole 28. Upper lead 24′ is then bonded, as with a eutectic bonding procedure, to the upper side of dielectric plate 18, preferably with a preformed hole 32 being aligned with hole 28 of dielectric plate 18. Solder 30 is then melted into holes 28 and 32 so as to form a conductive link between emitter electrode 24 and emitter lead 24. Further details of suitable conducting-through holes are discussed, for example, in an article by J.F. Burgess, C.A. Neugebauer, G. Flanagan and R.W. Moore, entitled "Hybrid Packages by the Direct Bonded Copper Process", Solid State Technology, May 1975, pages 42–44 (see Fig. 5 and discussion thereof). This article is hereby incorporated by reference.

Referring again to Fig. 1, interior electrodes 20, 22 and 24 of upper package section 12 are patterned to correspond to the upper terminals of power chip 16, which, as illustrated in exaggerated form for a power Darlington transistor, comprise a first base terminal (not shown) corresponding to interior electrode 20 of upper package section 12, an emitter t rminal 34, and a second bas terminal 36.

Power chip 16 has a single collector terminal 38 on its low r side (at least for a Darlington transistor) and is adapted to electrically c ntact lower packag secti n 14. In the illustrated mbodiment of p w r chip package

10, lower package section 14 comprises a collector electrode 17, preferably formed from a metallic sheet, such as copper, with an exemplary upwardly projecting collector lead formed integrally with collector electrode 17 and, further, with an upward-facing, concave recess 17b for accommodating power chip 16 when hermetic power chip package 10 is assembled. In order to permit bonding of lower package section 14 to upper package section 12, upper section 12 is provided with a metallic sealing ring 42, bonded to the underside thereof and encompassing interior electrodes 20, 22 and 24. Metallic sealing ring 42 preferably comprises copper eutectically bonded to dielectric plate 18, although it may comprise a solderable layer formed, for example, by evaporation of copper onto the underside of dielectric plate 18.

In accordance with a preferred procedure of assembling hermetic power chip package 10, the upper terminals of power chip 16 (i.e., the first base terminal, not shown, and terminals 34 and 36) are soldered to interior electrodes 20, 22 and 24 with preformed layers of solder. Lower terminal 38 of power chip 16 is then soldered to collector electrode 17 with a preformed layer of solder and, at the same time, collector electrode 17 may be soldered to metallic sealing ring 42 of upper package section 12. Other assembly procedures for package 10 will be apparent to those skilled in the art, such as a procedure wherein collector electrode 17 is bonded to metallic sealing ring 42 by laser or electron beam welding. When a sequence of soldering operations is used, as in the presently-described assembly procedure, a hierarchy of decreasing solder melting temperatures, preferably limited to two, will ensure that previous solder bonds are not remelted.

When power chip 10 is assembled, it appears as shown in the cross-sectional view of Fig. 4, which is taken along line 4–4 of Fig. 1. As can be observed, in Fig. 4, collector electrode 17 of lower package section 14 encloses power chip 16 within upwardly-facing concave recess 17b and is bonded to metallic sealing ring 42 of upper package section 12 so as to hermetically seal power chip 16 in package 10.

Power chip 16, when assembled in hermetic power chip package 10, can be electrically tested without danger of overheating and destruction, since collector electrode 17 can be mechanically pressed against a heat sink (not shown) for withdrawing heat from power chip 16. Electrical access t the first base terminal (n t sh wn), second base terminal 36, and emitter terminal 34 of power chip 16 is pr vided via first bas lead 20′, second bas lead 22′, and emitter l ad 24′, respectively, on the surface of dielectric plat 18 (s e Fig. 2). Hermetic power chip packag 10 b n ficially is in building block form inasmuch as it comprises only a portion of a complete hermetic power chip package assembly (not shown), and, as such, provides an economical means for testing power chip 16 before incorporation thereof into a complete, hermetic power chip package assembly. Of particular interest is the lack of a metallic baseplate in package 10.

If electrical isolation is desired between collector electrode 17 and a heat sink (not shown) upon which hermetic power chip package 10 is to be mounted, a further dielectric plate 44 as illustrated in Fig. 5 can be provided in bonded relationship to the underside of collector electrode 17 of power chip package 10. In the hermetic power chip package of Fig. 5, dielectric plate 44 preferably has a thermal expansion coefficient close to that of power chip 16 and suitably comprises the ceramic beryllia or alumina where power chip 16 comprises silicon. Dielectric plate 44 may be conveniently bonded to a metallic heat sink (not shown) via a metal layer 46 on the underside of dielectric plate 44, which preferably comprises copper eutectically bonded to dielectric plate 44, or alternatively, a solderable layer, such as evaporated copper. Collector electrode 17 is preferably bonded to dielectric plate 44 with a eutectic bonding procedure although collector electrode 17 could alternatively be soldered to a solderable metal layer (not shown), such as evaporated copper, provided atop dielectric plate 44.

Turning now to Fig. 6, there is shown a hermetic power chip package 60 looking upward towards package 60, in accordance with a further embodiment of the invention. Package 60 comprises an upper package section 12′ and a power chip 16′, which are suitable identical to upper package section 12 and power chip 16, respectively, of power chip package 10 of Fig. 1. Like reference numerals as between Fig. 6 and Fig. 1 refer to like parts.

Hermetic power chip package 60 further includes a lower package section 62 and a gasket 64 situated between upper and lower package sections 12′ and 62, respectively. Lower package section 62 comprises a collector electrode 66 with an exemplary collector lead 66a formed integrally therewith. If dielectric isolation of collector electrode 66 with respect to a metallic heat sink (not shown) is desired, lower package section 62 further includes a dielectric plate 68, such as the ceramic beryllia or alumina, with collector electrode 66 bonded to the upper surface of dielectric plate 68, preferably by a eutectic bonding pr cedur as discuss d above. Gask t 64 preferably comprises a material having a th rmal xpansi n c fficient within ab ut ± 50 p rcent of that of upper package secti n 12′. Wher p wer chip 16 comprises silicon, for example, gasket 64 suitably comprises molybdenum or tungsten, by way f

xample.

The interfitting of the various portions of power chip package 60 can be best appreciated by considering Fig. 7, which is a cross-sectional view of package 60 taken along lines 7–7 of Fig. 6. As is shown, the upper side of gasket 64 is bonded to metallic sealing ring 42′ of upper section 12′, and the lower side of gasket 64 is bonded to metallic sheet 66 of lower package section 62. Gasket 64 encompasses power chip 16′. It can be appreciated from Fig. 2 that dielectric plate 68 of lower package section 62 is wider and larger than collector electrode 66. This is to provide an elongated, so-called "electrical creep" distance on the surface of dielectric plate 68 between collector electrode 66 and a metallic baseplate (not shown) upon which dielectric plate 68 is typically mounted.

In accordance with a preferred procedure for assembling power chip package 60, power chip 16′ is first soldered to interior electrodes 20′, 22′ and 24′ of upper package section 12′ with a preformed layer of solder. Gasket 64 is then soldered to sealing ring 42′ of upper package section 12′ with a preformed layer of solder and lower package section 62 is simultaneously soldered to both lower terminal 38′ of power chip 16′ and to the lower side of gasket 64 with preformed layers of solder. As will be apparent to those skilled in the art, the foregoing sequence of soldering operations can be carried out by using preformed layers of solder, to limit to two, with a hierarchy of decreasing melting temperatures, so as not to impair solder bonds once formed.

Hermetic power chip package 60 achieves a high degree of mechanical integrity and is thus suitable for use under repeated cycling of power chip 16′ between widely differing heat and cold temperature (e.g., between −40°C and +150°C) because gasket 64 expands and contracts horizontally with dielectric plate 12′.

In an alternative embodiment of hermetic power chip package 60, a gasket 64′ as illustrated in Fig. 8 is provided in lieu of gasket 64 shown in Fig. 6. Gasket 64′ comprises a dielectric material preferably having a thermal expansion coefficient within about ±50 percent of that of dielectric plate 18′ (Fig. 7). Dielectric material 70 may suitably comprise the ceramic beryllia or alumina where power chip 16′ comprises silicon, for example. Solderable metal layers 72 and 74 are bonded to the upper and lower surfaces of gasket 64′, respectively, and preferably comprise eutectically bonded copper.

In providing a complet herm tic pow r chip package assembly (not illustrated), one or more of the foreg ing, hermetic power chip packages may be mount d, as by sold ring, to a metallic baseplate (n t shown). Such metallic baseplate may advantageously have mounted thereon "signal", or non-power, chips in their customary packages, that is, in signal chip carriers, resulting in a hybrid package. An inexpensive, non-hermetic housing may then be provided covering the metallic baseplate and both a hermetic power chip package(s) and a signal chip carrier(s), with provision for external electrical leads connected to the electrical leads of the enclosed hermetic power chip package(s) of signal chip carriers.

The foregoing describes hermetic power chip packages in building block form that permit economical testing of power chips and have a high capacity for waste heat removal from the power chips. In one embodiment, dielectric isolation is provided between a hermetic power chip package and a metallic heat sink on which the package is typically mounted.

While the invention has been described with respect to specific embodiments, many modifications and substitutions thereof will be apparent to those skilled in the art. It is, therefore, to be understood that the following claims are intended to cover all such modifications and substitutions as fall within the true spirit and scope of the invention.

CLAIMS

1. A hermetic power chip package, comprising:

a) an upper package section comprising a dielectric plate, at least a first electrode bonded to a lower surface of said plate and a first metallic lead bonded to an upper surface of said plate, at least one conducting-through hole in said dielectric plate electrically interconnecting said first electrode and said first metallic lead, and a metallic sealing ring bonded to the lower side of said plate and encompassing said first electrode;

b) a power chip including at least a first terminal located on an upper side thereof and bonded to said first electrode of said upper package section and further including a single terminal on a lower side thereof; and

c) a package lower section comprising a power chip lower electrode in sheet form bonded to said single terminal on the lower side of said power chip, said power chip lower electrode also being bonded to said metallic sealing ring of said upper package section so as to hermetically enclose said power chip.

2. The hermetic power chip of claim 1 wherein said first electrode and said first metallic lead each comprises copper that is eutectically bonded to said dielectric plate.

3. The hermetic power chip package of claim 2 wh rein said metallic sealing ring f said package upper section comprises copper that is eutectically bond d t said di lectric plat .

4. The herm tic power chip packag of claim 1 wherein said package lower s ction further comprises a diel ctric plate bonded to

the underside of said power chip lower electrode and a metallic sheet bonded to the underside of said dielectric plate.

5. A hermetic power chip package, comprising:

a) an upper package section comprising a dielectric plate, at least a first electrode bonded to a lower surface of said plate and a first metallic lead bonded to an upper surface of said plate, at least one conducting-through hole in said dielectric plate electrically interconnecting said first electrode and said first metallic lead, and a metallic sealing ring bonded to the lower side of said plate and encompassing said first electrode;

b) a power chip having at least a first terminal located on an upper side thereof and bonded to said first electrode of said upper package section and having a single terminal on a lower side thereof;

c) a package lower section comprising a power chip lower electrode in sheet form bonded to said single terminal on the lower side of said power chip, and

d) a gasket with upper and lower sides and encompassing said power chip, said upper side being bonded to said metallic sealing ring of said package upper section and said lower side being bonded to said power chip lower electrode of said package lower section so as to hermetically enclose said power chip.

6. The hermetic power chip package of claim 5 wherein said gasket has a thermal expansion coefficient within about ± 50 percent of that of said dielectric plate of said upper package section.

7. The power chip package of claim 5 wherein said power chip comprises silicon and said gasket comprises one of the group consisting of tungsten and molybdenum.

8. The power chip package of claim 5 wherein said gasket comprises a ceramic with upper and lower layers of copper being eutectically bonded to upper and lower surfaces of said gasket, respectively.

9. The power chip package of claim 5 wherein said first electrode and said first metallic lead each comprises copper that is eutectically bonded to said dielectric plate of said upper package section.

10. The hermetic power chip package of claim 9 wherein said metallic sealing ring of said package upper section comprises copper that is eutectically bonded to said dielectric plate of said package upper section.

11. The hermetic power chip package of claim 5 wherein said package lower section furth r c mprises a dielectric plat bond d to th underside of said power chip low r electrod and a metallic sheet bonded to the underside f said dielectric plate.

12. A hermetic pow r chip package substantially as h r in d scribed with reference to the acc mpanying drawings.

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